UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/813,866	03/22/2001	Kiichi Hirano	107318-00000	6213

7590 04/01/2002

ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
SUITE 600
1050 CONNECTICUT AVENUE
WASHINGTON, DC 20036-5339

EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/01/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Applicati n No.	Applicant(s)	
	09/813,866	HIRANO ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *44-59* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-59* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 44, 45, 52, 53, 54 and 55, are rejected under 35 U.S.C. 103(a) as being unpatentable Ohtani et al US patent No. 5,854,096 in view of Rohatgi et al US patent No. 5,766,964.

Ohtani teaches a method of fabricating a semiconductor device particularly a thin film transistor, comprising the steps of: forming an amorphous silicon film on an insulating substrate 11; heat treating said amorphous silicon film by laser annealing, therein forming a polycrystalline silicon film 104; forming an impurity regions 108/109 in said polycrystalline silicon film; rapidly heat treating the impurity region by rapid thermal annealing (RTA) using laser beam and laser lamp as a heat source for rapidly heat-treating the impurity region to activate the impurity region (figs. 3a to 3e, column 13, lines 49-59 and columns 19, lines 16-39).

Ohtani does not teach the use of xenon arc lamp for activating impurity region.

It would have been obvious to one of ordinary skill in the art to use xenon arc lamp as heat source in thermal annealing since xenon arc lamp is widely used in semiconductor processing.

Ohtani does not teach explicitly the limitation that the process step of rapid thermal annealing is performed a plurality of times while the heating temperature is increased stepwise from an initial time to a final time.

Rohatgi teaches RTA process conducted as claimed (column 8, lines 25-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching from Rohatgi in to the process steps of Ohtani since slowly ramping the temperature helps for a slow diffusion of impurities in to the silicon.

Regarding claim 46, Ohtani teaches substantially the entire claimed process as in claim 44 above including forming the gate electrode on the polycrystalline silicon film before the step of forming the impurity region in the polycrystalline silicon film (fig. 3a to 3e).

Regarding claim 49, Ohtani teaches substantially the entire claimed process as in claim 44 above including the amorphous silicon film contains microcrystals (column 1, lines 22-68).

Regarding claim 51, Ohtani teaches substantially the entire claimed process as in claim 44 above including the light irradiation heat from the lamp is employed as a heat source for the rapid thermal annealing (column 14, lines 13-37).

Regarding claim 59, Ohtani teaches substantially the entire claimed process as in claim 44 above except explicitly stating that applying laser annealing is performed by a laser beam in the form of sheet.

The shape of the beam is a matter of design choice. It would have been obvious to one of ordinary skill to in the art at the time the invention was made to come up with the laser beam shape as claimed in order to crystallize a specific area. In re Daily, 317 F.2d 699, 149 USPQ 47 (CCPA 1966).

Claim 47, is rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani in view of Sekine et al. US patent No. 5,937,300.

Regarding claim 47, Ohtani teaches substantially the entire claimed process as in claim 44 above except explicitly stating that the gate electrode comprises amorphous silicon where the amorphous silicon is crystallized by heat treatment during activation of the impurity region.

Sekine teaches a gate electrode comprising amorphous silicon (fig. 7a to 7c). Sekine does not explicitly teach the crystallization of amorphous silicon during RTA processing.

It would have been obvious to one of ordinary skill in the art to incorporate the process step of Sekine in to the method of Ohtani in order to form a semiconductor device since the process step described above cuts the fabrication time.

Claims 48 and 50, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani in view of Sekine.

Ohtani teaches substantially the entire claimed process as in claim 44 above except explicitly stating that gate electrode has a layered structure of a silicon film and one of a metal and metal silicide film, and reduction of resistance of the gate electrode

and activation of the impurity region are simultaneously performed by one of rapid thermal annealing and laser annealing.

Ohtani teaches the use of rapid thermal annealing and laser annealing for activating ion-implanted impurities in the process of making thin film transistor. Ohtani does not teach a gate electrode comprising the claimed material above.

Sekine teaches a gate electrode comprising a silicon film, a metal film and a metal silicide in the process of making for making semiconductor device (fig. 7a-7c).

It would have been obvious to one of ordinary skill in the art to incorporate the process steps from Sekine in to the method of Ohtani since forming silicide as a gate electrode is known to reduce the resistance of the gate electrode.

Claims 56, 57 and 58, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ohtani.

Regarding claims 56 and 58, Ohtani teaches a method of fabricating a semiconductor device, comprising the steps of: forming a semiconductor film on a substrate 501; forming a gate electrode 505 on the substrate on a gate insulating film 504; forming an impurity regions 506 and 507 in the semiconductor film; and activating the impurity region by a heat treatment through rapid thermal annealing (figs 5a-5d).

Ohtani does not explicitly teach heating by the rapid thermal annealing being performed a plurality of times where the heating temperature being increased stepwise from an initial time to a final time.

Ohtani does not teach explicitly the limitation that the process step of rapid thermal annealing is performed a plurality of times while the heating temperature is increased stepwise from an initial time to a final time.

Rohatgi teaches RTA process conducted as claimed (column 8, lines 25-45).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching from Rohatgi in to the process steps of Ohtani since slowly ramping the temperature helps for a slow diffusion of impurities in to the silicon.

Regarding claim 57, Ohtani teaches substantially the entire claimed process as in claim 56 above including the highest heating temperature in the stepwise increment in temperature through rapid thermal annealing is a temperature not deforming the substrate (column 19, lines 27-39).

Conclusion

2. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-H are cited as being related to thin film transistors.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Samuel Admassu Gebremariam
March 25, 2002

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800